Digitally Programmable Current-Mode Analog Fuzzy Membership Function Circuit

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Key Word - I *Fuzzy Hardware*

Key Word - II *Fuzzy Membership, Membership Function, Fuzzy Logic, Fuzzy Systems, Hardware Implementation, Circuit Design, VLSI Design, Hybrid Architectures, Adaptive Fuzzy Control, Fuzzy Control, Parallel Processing, Parallel Implementations, Set Membership, Fuzzy Sets, Data Fusion*

Abstract

A digitally programmable current-mode analog fuzzy membership function circuit (MFC) has been designed, simulated and fabricated in a $0.5\mu m$ CMOS technology. The MFC implements a generalized trapezoidal membership function with both normal and complement outputs. The right and left leg positions are each specified by 8-bit numbers while the right and left slopes are digitally programmable to thirty-one evenly spaced values by using a novel 5-bit dividing digital to analog converter (DivDAC). V-I and I-V front and back ends allow for internal current-mode analog operations which are low-power, high-speed, and area efficient. The MFC's versatility is increased by using bias currents and voltages to allow the specification of maximum-membership voltage levels as well as input and output DC offsets. The entire circuit including memory measures $49\mu m \times 1234\mu m$ and is capable of fuzzification in less than $600ns$ while consuming $5.3\mu W$.

1 Introduction

The Ballistic Missile Defense Organization (BMDO) is conducting the Discriminating Interceptor Technology Program (DITP) for the development of advanced fast frame seeker capabilities. This effort includes research into new sensor data fusion processing technologies that address high speed and on-board autonomy with serious space, weight, and power constraints[1]. Fuzzy logic is one of several modes of processing being investigated[2]. The stringent requirements dictate the use of dedicated fuzzy hardware in order to achieve the necessary low-power, fast processing, and compact implementation.

Digital approaches to fuzzification[3, 4, 5] offer a high degree of noise immunity along with specifiable levels of precision and flexible programmability. High precision however is not necessarily required for fuzzy processing since fuzzy classes are usually defined by humans with less than 8-bits of resolution. The relatively large layout area of digital circuits makes it more difficult to take advantage of the increased throughput achievable from the inherently parallel nature of fuzzy computations. This combined with the higher dynamic power consumption of digital circuits makes a digital approach less suitable for meeting the DITP goals.

Analog approaches to building membership function circuits (MFCs) offer advantages in speed, compactness, and low power, but tend to be difficult or inflexible to configure. Many of the circuits in the literature[6, 7, 8, 9, 10, 11] require bias voltages and transistor geometry changes to achieve different membership function positions and shapes. In systems requiring many membership functions this configuration technique is impractical due to pin and supply limitations.

Huertas *et al.*[12] present a mixed-mode approach that offers the flexibility of digital programming with the speed, compactness, and low power of current-mode analog CMOS. Their hybrid MFC, however, is limited to a strictly symmetrical trapezoid and offers only four different multiplicative slope values. The hybrid current-mode approach offers a high degree of functional efficiency since the basic required operations of subtraction and addition can be performed easily at node junctions. The MFC presented in this paper builds upon the hybrid approach by adding programmable versatility at the expense of increased circuit area.

2 Membership Function Circuit

The membership function circuit presented here creates a trapezoidal DC transfer function with programmable parameters for the leg positions and slopes as illustrated in Figure 1. The position of the legs can be specified with 8-bit resolution and the slopes with 5-bit resolution. Our generalized trapezoidal membership function is described by the following equations:

$$\begin{aligned}
x \leq A \quad &\Rightarrow \quad y = Low \\
A < x \leq \frac{(CD + AB)}{(B + C)} \quad &\Rightarrow \quad y = \min(Bx - AB + Low,\ High) \\
\frac{(CD + AB)}{(B + C)} < x < D \quad &\Rightarrow \quad y = \min(-Cx + CD + Low,\ High) \\
x \geq D \quad &\Rightarrow \quad y = Low
\end{aligned}$$

where A is the location of the left leg, B is the unsigned slope of the left leg, C is the unsigned slope of the right leg, and D is the location of the right leg. The chip design presented in Section 4 currently uses Low = 3V and $High$ = 5V with Vdd = 5V.

Figure 2 details the processing path of a single membership function circuit (MFC). While inputs and outputs are in voltage mode for external compatibility, the internal MFC implementation is in current-mode for easy and compact signal manipulation. The input voltage enters a voltage to current

(V/I) converter in the first processing block. Currents proportional to the digital values of the leg positions, A and D, are generated by digital to analog converters (DACs). The current corresponding to the left leg gets subtracted from a copy of the input current while a different copy of the input current gets subtracted from the right leg current. The resulting currents, which correspond to the left and right sides of the trapezoid, enter their appropriate dividing digital to analog converters (DivDACs)[13] where the signals are divided by 5-bit digital values to scale the slopes. The minimum of the two resulting values is then selected, which determines the appropriate side of the trapezoid at the given input level. The top of the trapezoid is achieved by limiting the previously resulting current to an externally supplied full-scale current. The final output current is then converted to the voltage output and complement output of the MFC through current to voltage (I/V) converters.

Typical hybrid multipliers, often referred to as multiplying digital to analog converters (MDACs), are often useful in mixed-mode systems since they provide a programmable multiplication of an analog signal by a digital number. This technique has previously been used to scale the slope of membership functions[12]. The novel DivDAC circuit[13] developed at JPL, however, allows for digital programming of the *denominator* as opposed to the numerator, which proves to be much better at generating useful slopes. Figure 3 shows the difference in programming utility between changing the numerator versus the denominator for the desired slope range in the MFC. With multiplication, the slopes bunch up towards the vertical range limit as seen in Figure 3b and in [12], whereas with division they are evenly spaced throughout the range of interest.

3 CMOS Implementation of the MFC

The voltage to current converter in the input stage is based on the COMFET circuit in [14]. This differential circuit provides V/I gain control as well as good linearity in a wide DC operating range.

The differential current outputs of the V/I, I_1 and I_2, are routed to the current subtracters shown in Figure 4. I_L generated by the left 8-bit DAC is sunk from a common node with I_1 being sourced in and I_2 being sunk out such that KCL dictates that the resultant current is $I_{in} - I_L$, where $I_{in} = I_1 - I_2$. Similarly for the right side, I_R from the right DAC is sunk out of a common node with I_{in} being sourced, producing by KCL the current $I_R - I_{in}$. The currents $I_{in} - I_L$ and $I_R - I_{in}$ resulting from the subtracters are routed to the left and right DivDACs for slope scaling.

The DivDAC shown in Figure 5 was developed at JPL specifically for this application because of the need to program the membership function slopes through division. It shares the same basic current mirror architecture as most MDACs, such that the output current is determined by a ratio of transistor sizes. The gain of a current mirror can be expressed as:

$$\frac{I_{out}}{I_{in}} = \frac{(\frac{W}{L})_{output}}{(\frac{W}{L})_{diode}} \tag{1}$$

An MDAC switches the output devices, so that a digital number can specify the numerator in Eq. 1, thereby varying the MDAC's gain. In the DivDAC, however, the switches are placed on the diode side of the current mirror, allowing digital control of the *denominator.* Because of the potential for the series resistance of a switch to adversely affect the IV characteristics of a diode connected transistor, the switches were placed on the gate of each device, rather than in series with each device.

The left and right output currents of the DivDACs, I_{LDiv} and I_{RDiv} respectively, next enter the Selector Circuit shown in Figure 6. Current copies, one for comparison and one for output, are made for both sides in cascode mirrors. The currents are compared at a common drain node S, which is pulled down towards ground if I_{LDiv} is larger, and pulled up towards Vdd if

I_{RDiv} is larger. The voltage at node S is buffered and inverted and used to control PMOS switches to select and pass whichever current is smaller. This determines the appropriate side current of the trapezoid, I_{Side}.

To achieve maximum membership clipping, and thus a trapezoidal shape rather than a triangle of variable height, a limiter circuit is employed as shown in Figure 7. The circuit also includes some gain in order to scale the current up for the output stage. The limiting is achieved by tying the source node of a cascode mirror to an NMOS limiting transistor whose gate is set to carry a fixed current. The voltage at this source node then rises to limit the current passed through another gain stage to the output stage. Note that since I_{Limit} includes the cascode diodes, the maximum output current as designed in Figure 7 is set at:

$$\frac{2}{3} \cdot I_{Limit} \cdot 8 = \frac{16}{3} \cdot I_{Limit}$$

Finally, the output stage shown in Figure 8 takes the current I_{out} generated by the limiter stage and adds an offset current I_{offset} so that the output DC bottom level can be set to a desired voltage value (in our case 1V). A cascode mirror then sinks this current across a $60k\Omega$ silicide blocked polysilicon resistor to generate the complement output voltage V_{out_comp} which is buffered through a voltage follower. The same current, $I_{out} + I_{offset}$, is also sourced through a PMOS cascode mirror across another $60k\Omega$ resistor to produce V_{out} through a voltage follower.

4 Hardware Results

The MFC was fabricated in an HP $0.5\mu m$ CMOS process through the *MOSIS* service. The test chip consisted of two input variables with five membership functions each. Each membership function was independently programmable but shared bias currents for the DACs, the input and output ranges, and the limiting level. Results of programming an MFC are shown in Figure 9 along with the complement outputs. The input range as tested was from 3V to 5V and the output range was set from 1V to 4V. The MFC's propagation delay and rise/fall time was measured to be under $600ns$ while consuming around $5.3\mu W$.

The MFC is intended to be placed in fully parallel fuzzy processing systems. As such, the layout was done to make the MFC long and flat in order for it to stack easily and compactly while sharing data and bias lines. Our particular test chip consisted of a stack of ten MFCs all capable of operating in parallel. Attention was given in the design to matching and consistency by using differential input currents and large geometry biasing devices. It should be noted, however, that we did not observe exactly similar behavior from the various MFCs on the chip due to process variation, which produces geometric mismatches as well as doping gradients that influence the threshold voltage as a function of location on the die. On the positive side, since our circuits were digitally programmable, we were able to compensate somewhat for these variations through programming and manipulation of the biases. Future designs should pay careful attention to minimizing the effects of process variation on circuit consistency.

5 Conclusion

We have demonstrated a fully programmable hybrid membership function circuit capable of implementing a generic trapezoid transfer function across a adjustable input and output voltage range. The circuit uses a novel 5-bit hybrid DivDAC to specify membership function slope through digital programming of the denominator as opposed to the numerator, giving better coverage of the desired slope range than MDAC approaches. The MFC was fabricated and tested, and results demonstrate the versatility of our hybrid approach. The MFC presented should enable highly parallel, high speed, low power fuzzy systems with a great degree of digitally programmable flexibility.

6 Acknowledgment

The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Ballistic Missile Defense Organization through an agreement with the National Aeronautics and Space Administration. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

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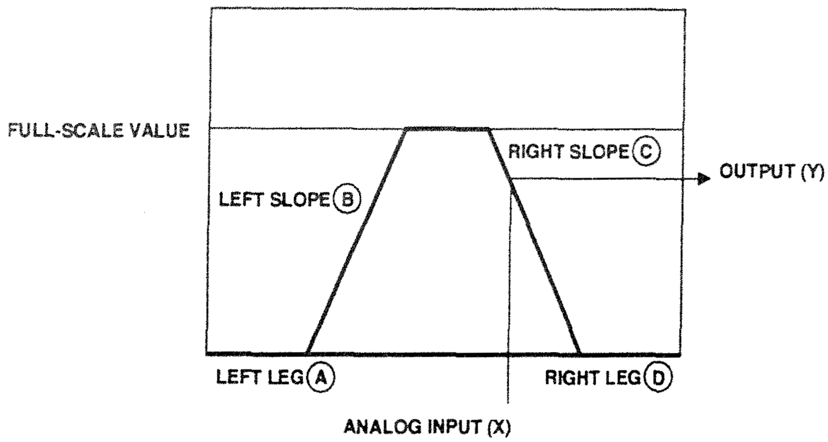


Figure 1: Generalized trapezoidal membership function showing MFC programming parameters.

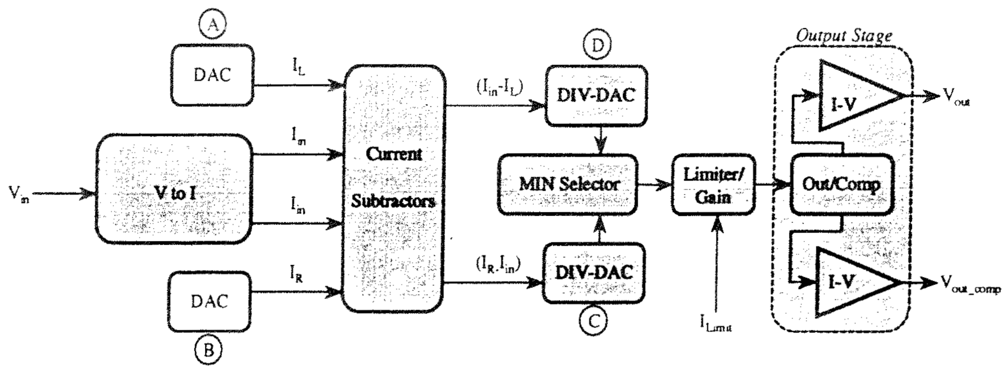
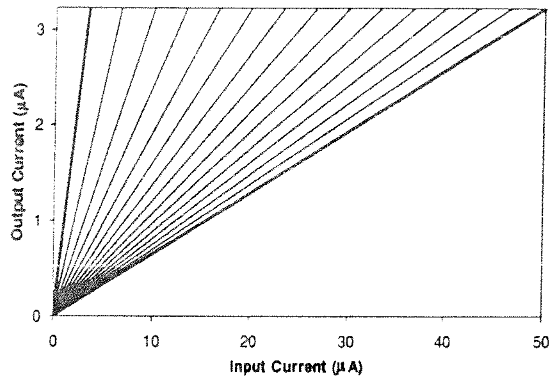


Figure 2: Block diagram of the membership function circuit (MFC).

a)



b)

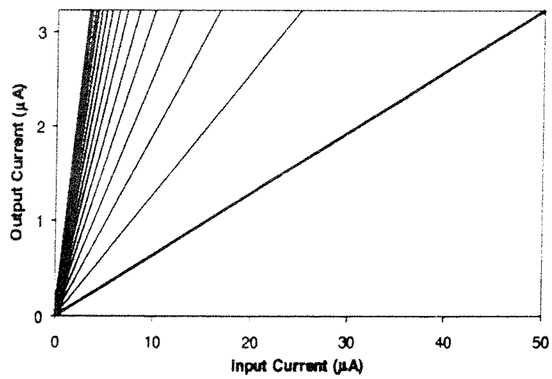


Figure 3: Programmable membership function slopes for n from 1 to 15: a) Using division where n is the denominator b) Using multiplication where n is the numerator.

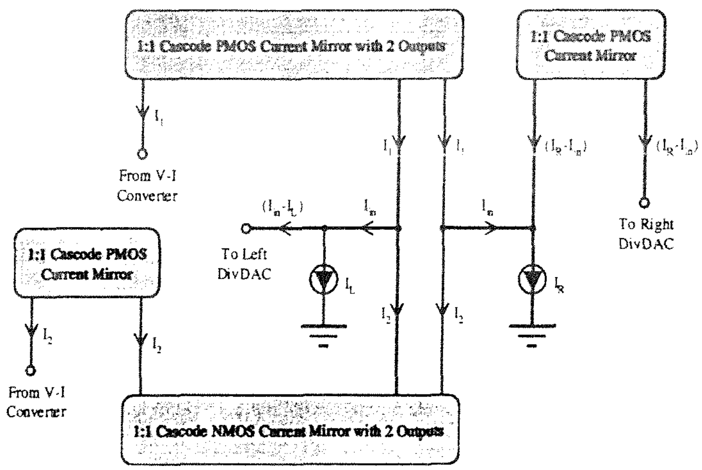


Figure 4: MFC circuitry from the V-I input stage to the slope-determining DivDACs. I_{in} is the difference of the V-I converter's output currents (I_1 and I_2). I_L and I_R are the output of 8-bit current-mode DACs.

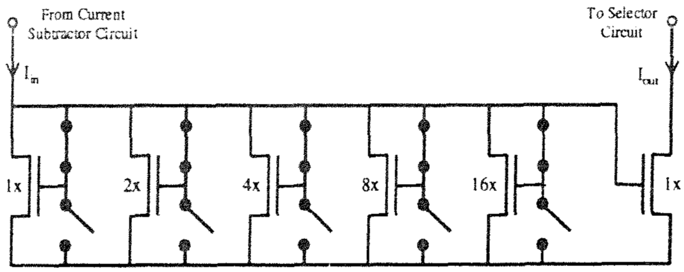


Figure 5: Simplified schematic of the 5-bit hybrid DivDAC circuit configured for division by 31.

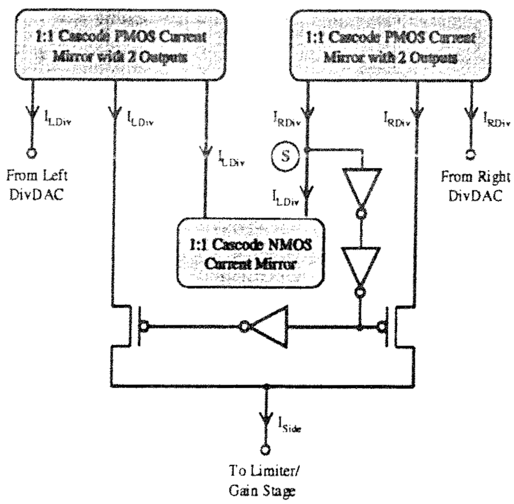


Figure 6: Selector Circuit. The output of each DivDAC is compared, and the smaller of the two is passed on to the clipping circuit.

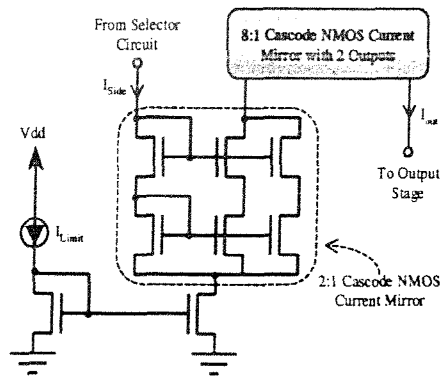


Figure 7: Limiter/Gain Stage: I_{out} is clipped at a max of $\frac{16}{3} \cdot I_{Limit}$.

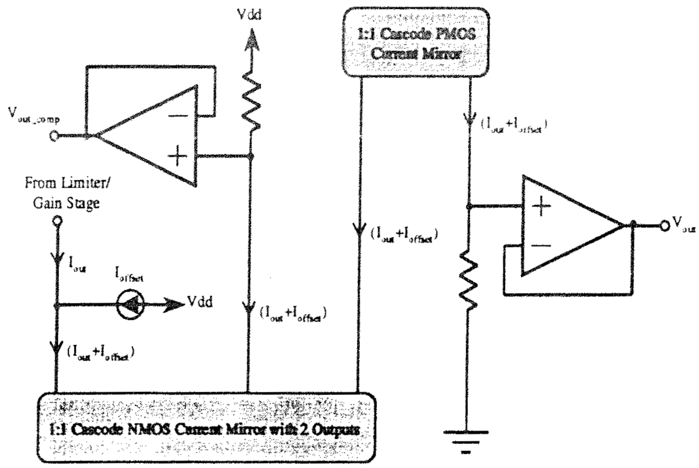


Figure 8: Output Stage: the final output voltage and its compliment are buffered before being sent off-chip.

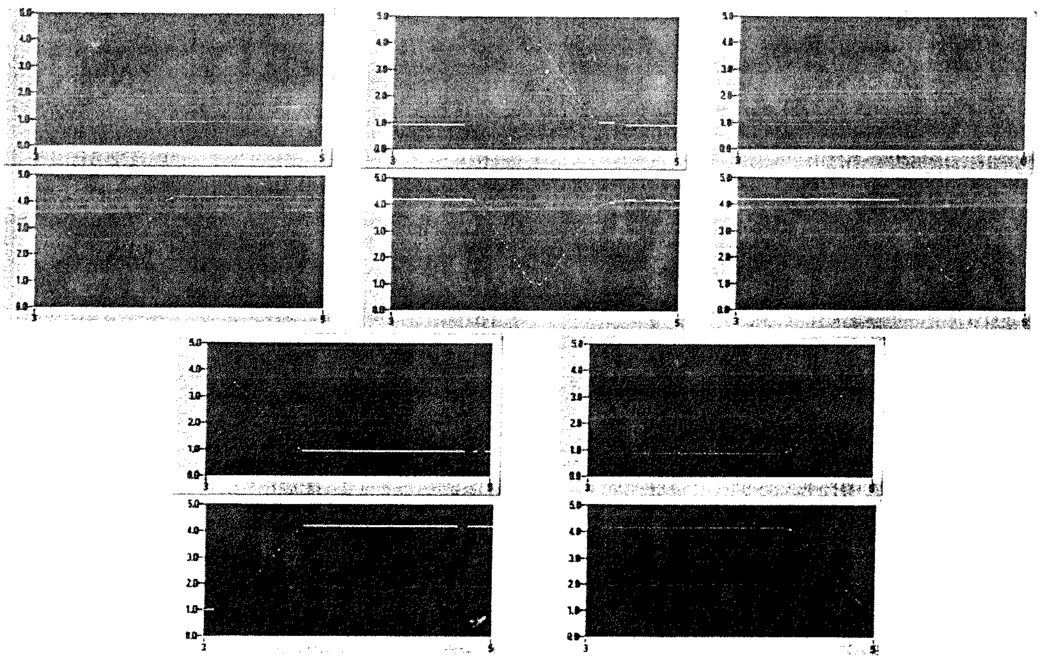


Figure 9: Voltage and complement voltage outputs of the fabricated MFC for different digital configurations.